cRIO OPIF 2Tx/2Rx Manual

Optical transceiver modules for Compact RIO

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DOCUMENT INFORMATION

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Revision history

Version	Date	Author	Change Log
1.0	17.04.2015	Michael Rost	First draft for 20Mbit/s version
2.0	07.02.2018	Michael Rost	Adapted to 5 and 20 Mbit/s versions including different connectors: SC, ST, FC, SMA

CONTENT

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1 Introduction

This document describes the optical interface module for Compact-RIO, which contains

- 2 optical Transmitters
- 2 optical Receivers

Both transmitters and receivers can be selected for different speed ranges

- 0...5 MBit/s
- ...20 Mbit/s (no static signalling)

Both transmitters and receivers can be selected for different fiber connector types:

- SC
- ST
- FC
- SMA

In the following chapters the hardware and the basic software drivers are highlighted.

1.1 Purpose of this document

Purpose of this document is to describe how to integrate the module in a test system and how to access it from the software point of view. Limits of application are shown in the technical data section.

This document is addressed to system integrators and the users, who are applying the module.

1.2 Definitions and abbreviations

Abbreviation	*Definition*
cRIO	**Compact RIO** (Measurement device platform of National Instruments
OPIF	**Op**tical **I**nter**f**ace
SPI	**S**erial **P**eripheral **I**nterface (clock synchronous data output)

1.3 References

Document	*Date*	*Description*
AV02-0176EN_DS_HFBR-x4xxZ_2014-11-18.pdf	08.11.2014	Optical transceiver data sheet

1.4 Document Overview

This documented contains 3 sections.

- The first section includes an introduction to this manual
- The second section includes description of the hardware
- The third section includes accessing the module from the software point of view.

2 Hardware

1.1 Overview

Following block diagram shows the hardware of the module:

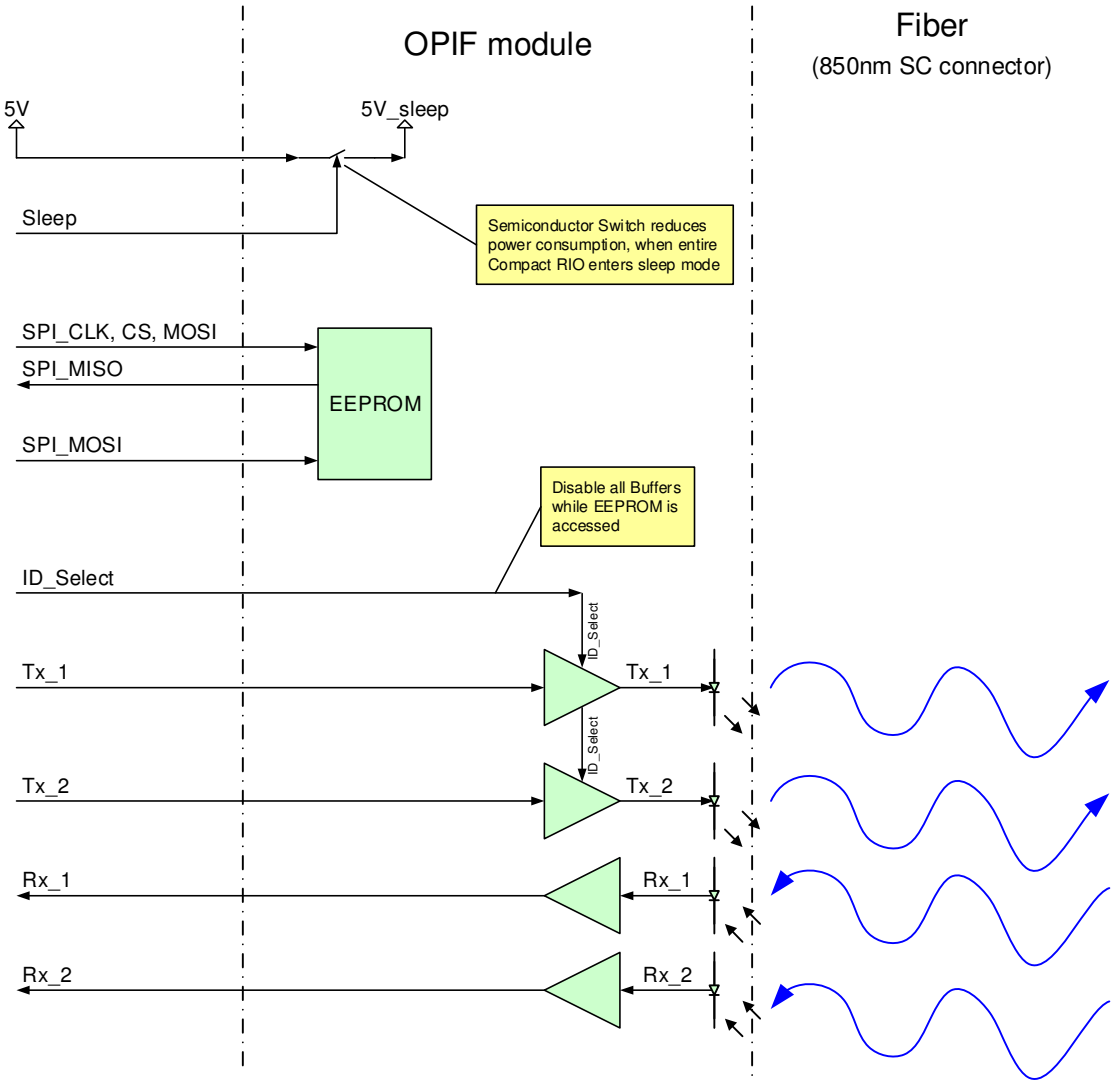


Figure 1: OPIF HW Overview

During **start-up or reset** of the Compact-RIO system the IOs between the optical interface module and the Compact-RIO are floating. The module is designed in this way, that the transmitter outputs do not emit light during startup phase. I.e. **NO LIGHT** should be regarded as the **SAVE STATE**.

In case of 20Mbit/s versions receivers may show an arbitrary level after power-up. After the first edge is detected, the level is well defined. I.e. The receivers show a logic high, when light is applied. They show low otherwise.

If the **EEPROM is accessed** from the Compact-RIO, all transmit Buffers are disabled. **No light is emitted** by the transmitters.

2.1 Dimensions

cRIO OPIF is designed in a standard Compact-RIO housing with the appropriate Sub-D-Connector. The transmitter and receiver optical IOs vary depending on connector type (SC, FC, ST or SMA)

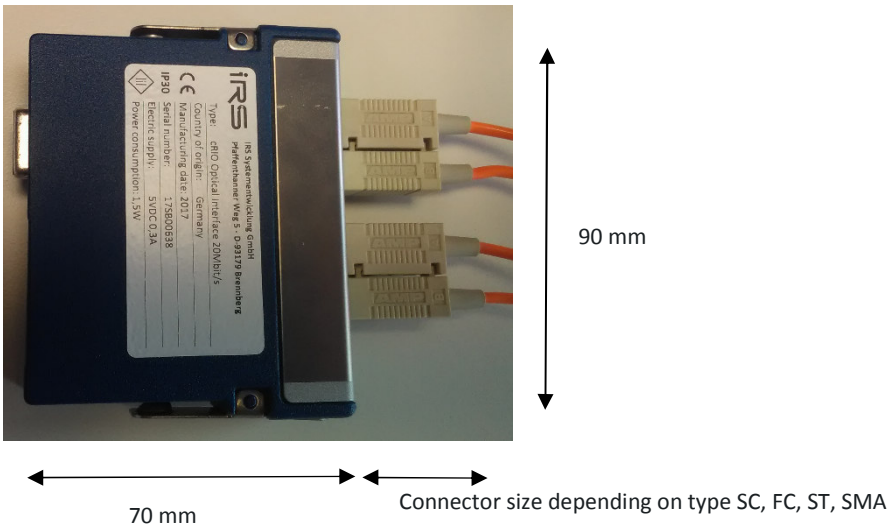


Figure 2: OPIF Dimensions

2.2 Technical data

Following table shows the technical data of the module.

Item	Min	Typical	Max	Unit
Ambient Temperature	0	25	50	°C
Supply Voltage (supplied by Compact-RIO)	4.75	5.0	5.25	V_{DC}
Supply current (all transmitters off)	100	150	200	mA
Baudrate		10	20	MBit/s
Forward current per transceiver (Light On, Logic level Low)		62		mA

2.2.1 Timing 20Mbit/s

Item	Min	Typical	Max	Unit
Data rate - no static signalling for 20Mbit/s!	**>0!**	10	20	MBit/s
Driver buffer propagation delay (between Compact-RIO and transmitter LED) additional to HFBR14E4Z		2	4	ns
Receiver buffer propagation delay (between Receiver and Compact RIO) additional to HFBR24E6Z		2	5	ns
Propagation delay through 2m fiber including all drivers and receivers (see also following figure)		25		ns

For detailed technical data of transmitters and receivers, refer to HFBR14E4Z / HFBR24E6Z datasheet

Following figure shows a timing example of a 20Mbit/s transmission. The shown signals are captured at the cRIO internal pins, which are directly accessed by LabVIEW FPGA. Please note, that you may add delay for synchronisation registers.

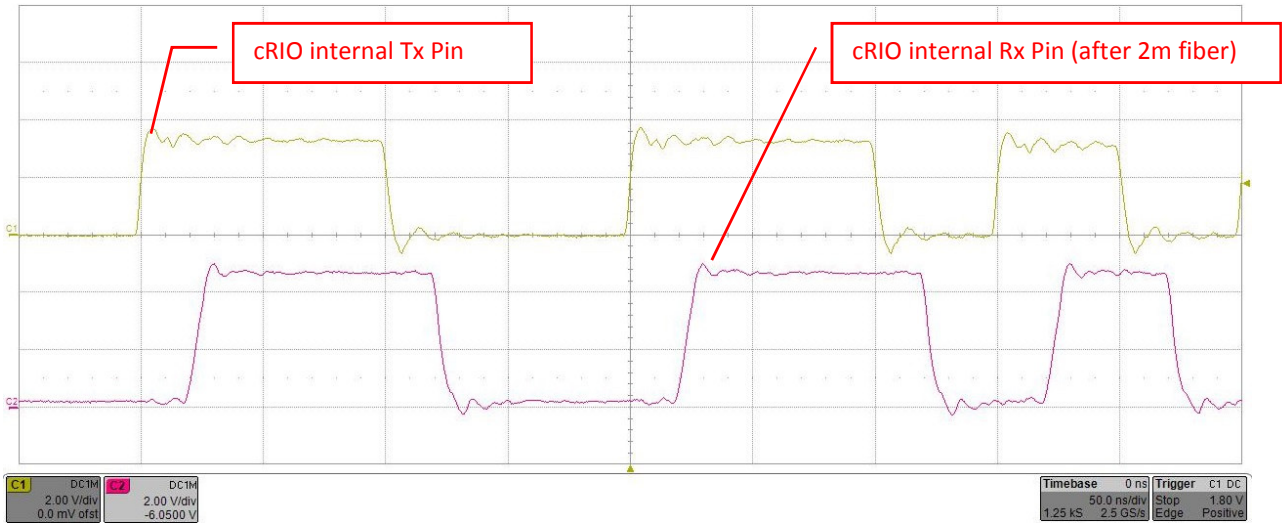


Figure 3: Timing 20Mbit/s

2.2.2 Timing 5Mbit/s

Item	Min	Typical	Max	Unit
Data rate	0		5	Mbit/s
Driver buffer propagation delay (between Compact-RIO and transmitter LED) additional to HFBR14x4Z		2	4	ns
Propagation delay through 1m fiber including all drivers and receivers @ Rising edge input (see also following figure)		100		ns
Propagation delay through 1m fiber including all drivers and receivers @ Falling edge input (see also following figure)		50		ns

For detailed technical data of transmitters and receivers, refer to HFBR14x4Z / HFBR24x2Z datasheet.

Following figure shows a timing example of a 5Mbit/s transmission. The shown signals are captured at the cRIO internal pins, which are directly accessed by LabVIEW FPGA. Please note, that you may add delay for synchronisation registers.

Please note also that receivers for 5Mbit/s add an inversion to the input signal. This inversion has to be considered in the software.

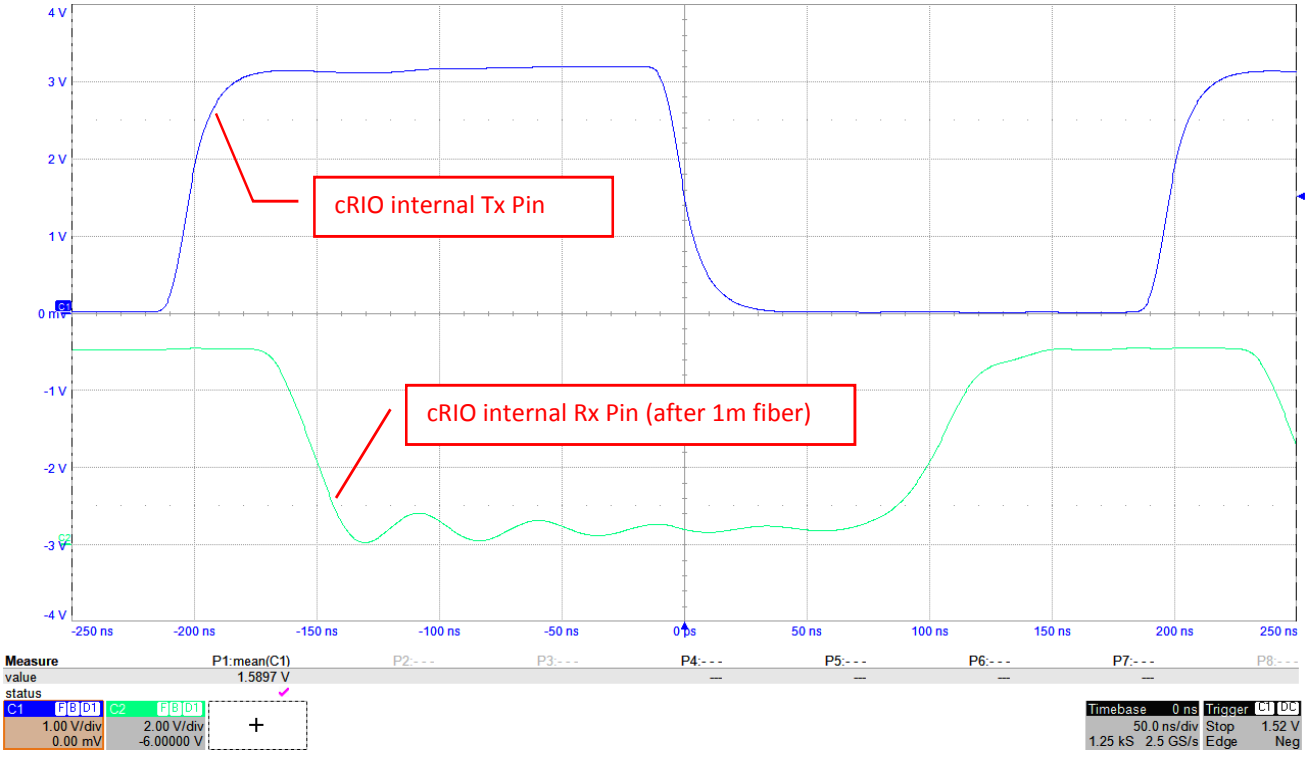


Figure 4: Timing 20Mbit/s

3 Software overview

In the following chapter the example projects are described. In the first example, the user is introduced, how to include the module into the user's application project.

3.1 Simple access example

The simple access example can run only on the Compact-RIO FPGA and may be started directly from the host-PC. The example is included in the documentation CD: "**cRIO_OPIF_Basic_Access**"

The example shows two buttons to control the Tx outputs of the module and two indicators, which show the status of the receiver inputs. The following figure shows the front panel, where the receiver inputs are directly connected to the transmitter outputs via plastic fibre.

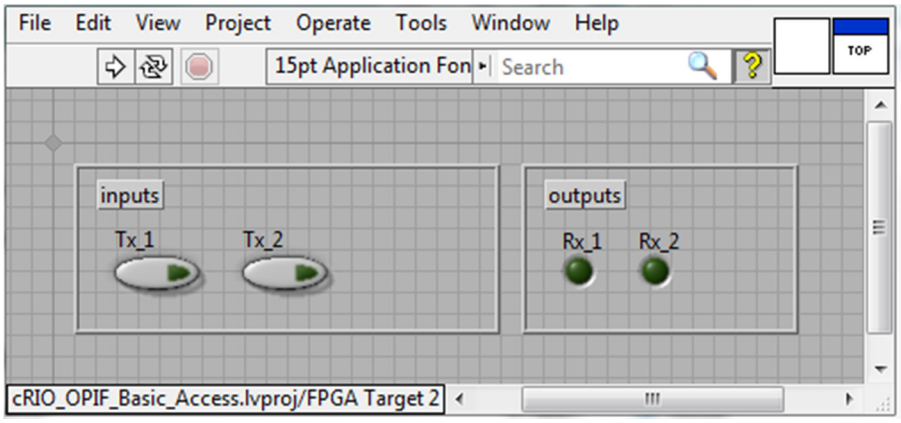
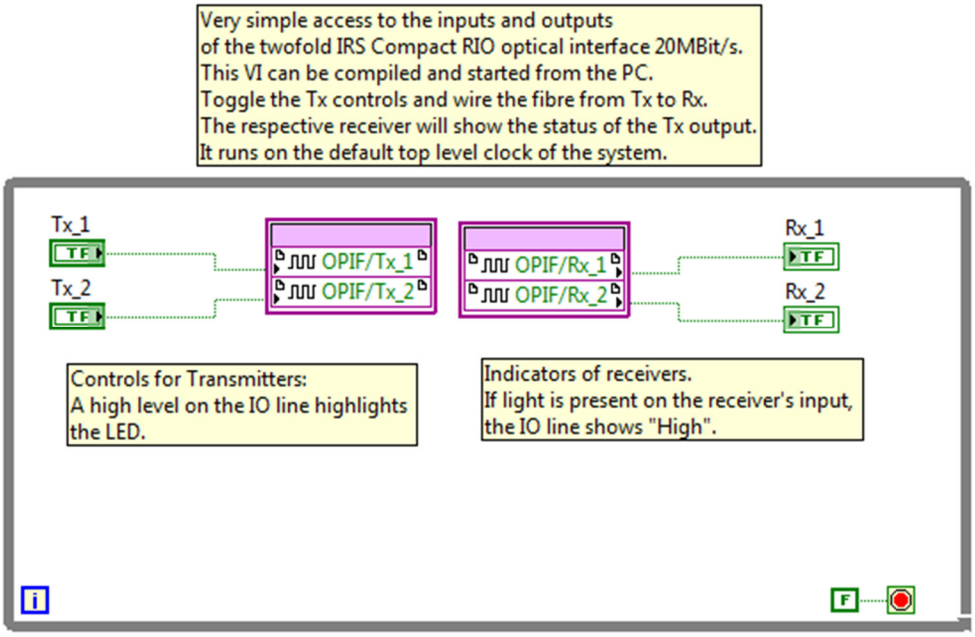


Figure 5: Simple access example front panel

The following block diagram illustrates, how the IO lines of the module can be directly accessed in the example, using read/write controls to the user and FPGA IO nodes to the module's hardware.



Please note, that for 5Mbit/s receiver signals are inverted!

Figure 6: Simple access example block diagram

The FPGA IO nodes have to be specified in the project as shown in the following figure:

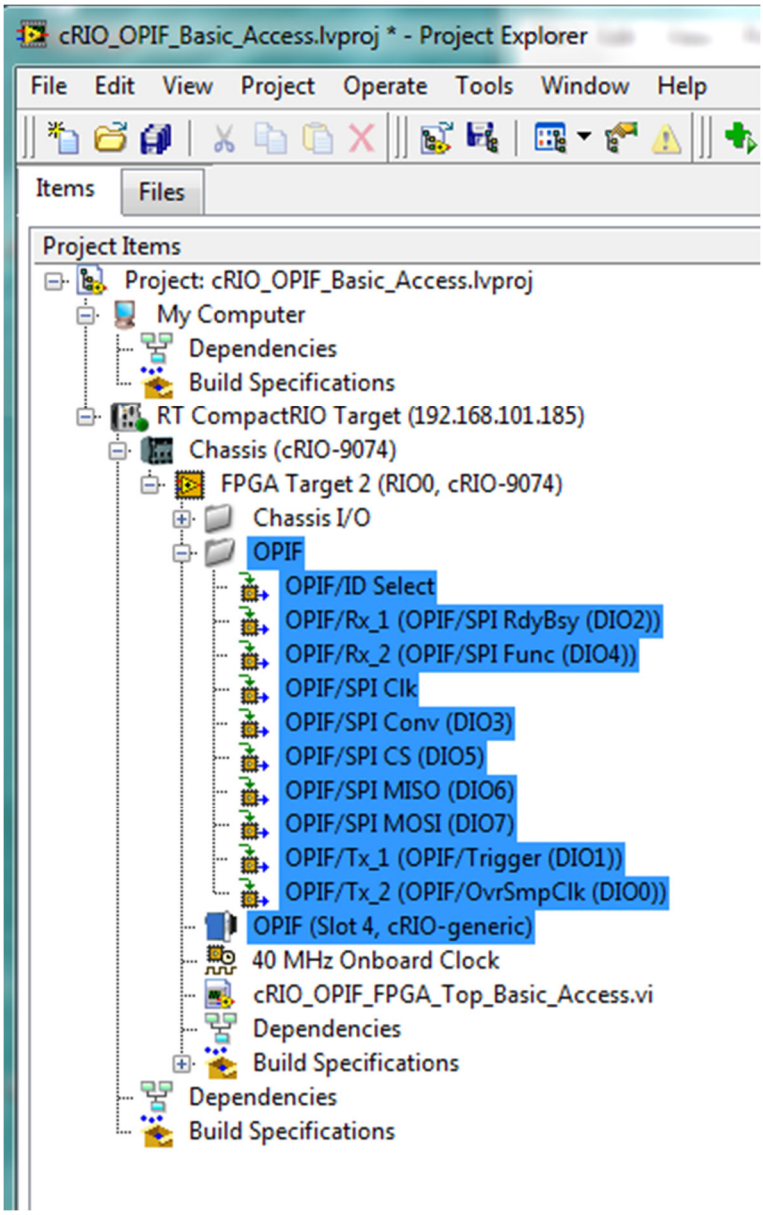


Figure 7: FPGA IO nodes

3.2 Including the module in the user application

To include the module into the user application the blue marked items of the previous figure have to be copied into the LabVIEW project of the user. There are some steps to perform after you have setup your LabVIEW project according to your applied Compact-RIO system:

First include a new cRIO device:

- **Right-click** on "**FPGA Target**"
- Select from Popup- Menu "**New->C Series modules…**"
- Select the checkbox "**New Target or Device**" in the following window:
- Select C Series Module and press "**OK**"

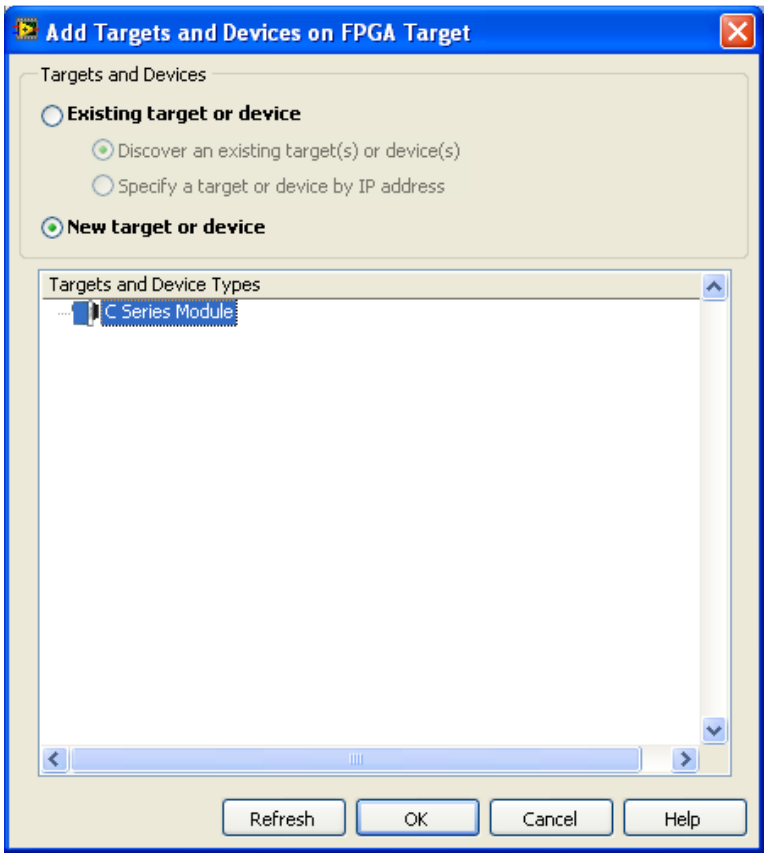


Figure 8: Add c-series module

The following window will appear.

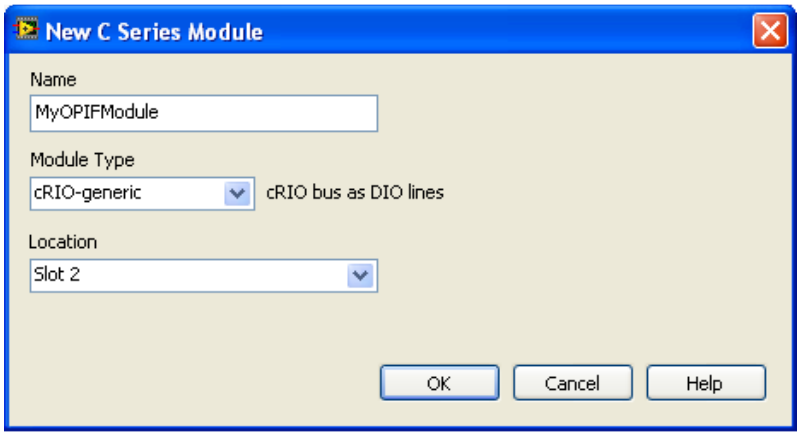


Figure 9: Select cRIO-generic type

Select

- an appropriate name for the module
- "**cRIO-generic**"
- the **Slot** of the Compact-RIO chassis, where the module should be applied.

Note: If the cRIO-generic module can't be selected, please include the following line into your "LabVIEW.ini" file, while LabVIEW is closed.

```
cRIO_FavoriteBrand=generic
```

Rename the IOs of the module according to the following table, where the respective Rx (Rx_1, Rx_2) and Tx channel (Tx_1, Tx_2) must fit to the respective DIO-line (DIO0…DIO7), which is shown automatically after the C-series module has been included

OPIF Signal	C-Series Module DIO line
SPI Clk	SPI Clk
ID Select	ID Select
Tx_2	DIO0
Tx_1	DIO1
Rx_1	DIO2
	DIO3 / SPI Conv
Rx_2	DIO4
SPI CS	DIO5 / SPI CS
SPI MISO	DIO6 / SPI MISO
Tx_1	DIO7

The Project window will appear similar to the figure ”Figure 7: FPGA IO nodes”.

Note, that you may also use different names of the signals.

If you want to apply several optical interface modules, you have to repeat the process as often as there are modules. In this case, the signal names of all modules must be unique in the whole project.

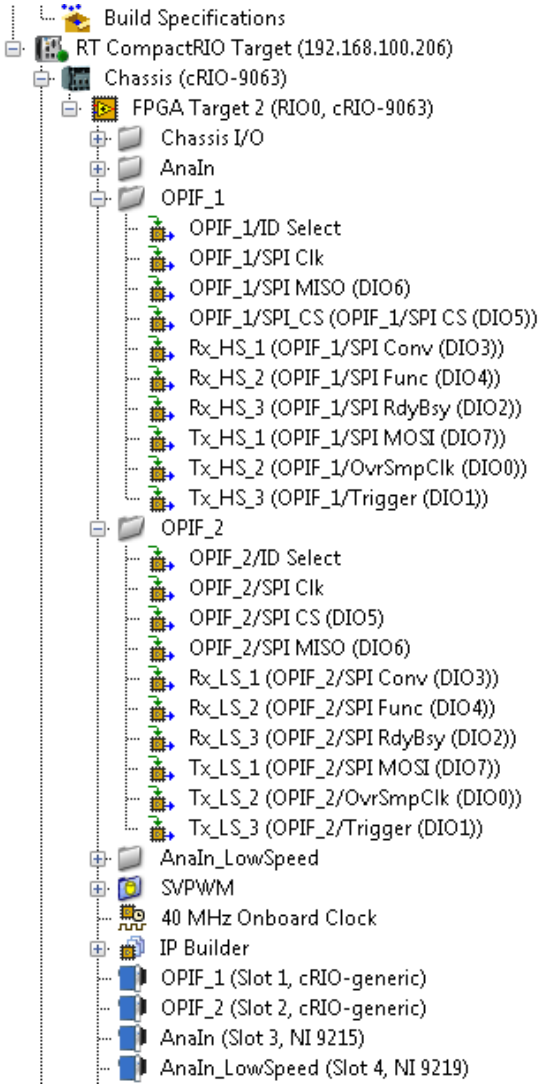


Figure 10: several modules in parallel

3.3 Bit error rate testing (20Mbit/s)

The following example generates a bit-stream in the FPGA, transmits the bit-stream on the optical transmitters, receives the data via the optical interconnected receivers and compares transmitted and received data to determine bit error rates of the transmission. The example is included in the documentation CD: "**cRIO_OPIF_BER-Test**"

In detail the example performs the following:

- The FPGA generates bit-streams for the transmitters continuously
- The bit-streams may be selected from three options
  - Static control (as in the basic access example)
  - Toggle (with every clock, the transmitter level changes its level)
  - Noise (uniform white noise with adjustable amplitude as 16 bit value)
- Transmitters should be optically connected to the receivers
  - Transmitter 1 to Receiver 2
  - Transmitter 2 to Receiver 1
- The received data is over-sampled at 80Mhz, where every second sample is valid. I.e. the real data sampling frequency is 20MHz, as it is the same as for the transmitters.
- The received data is compared with the transmitted data.

The following figure shows the example front panel of the PC software, which controls and visualizes the bit error rate tester:

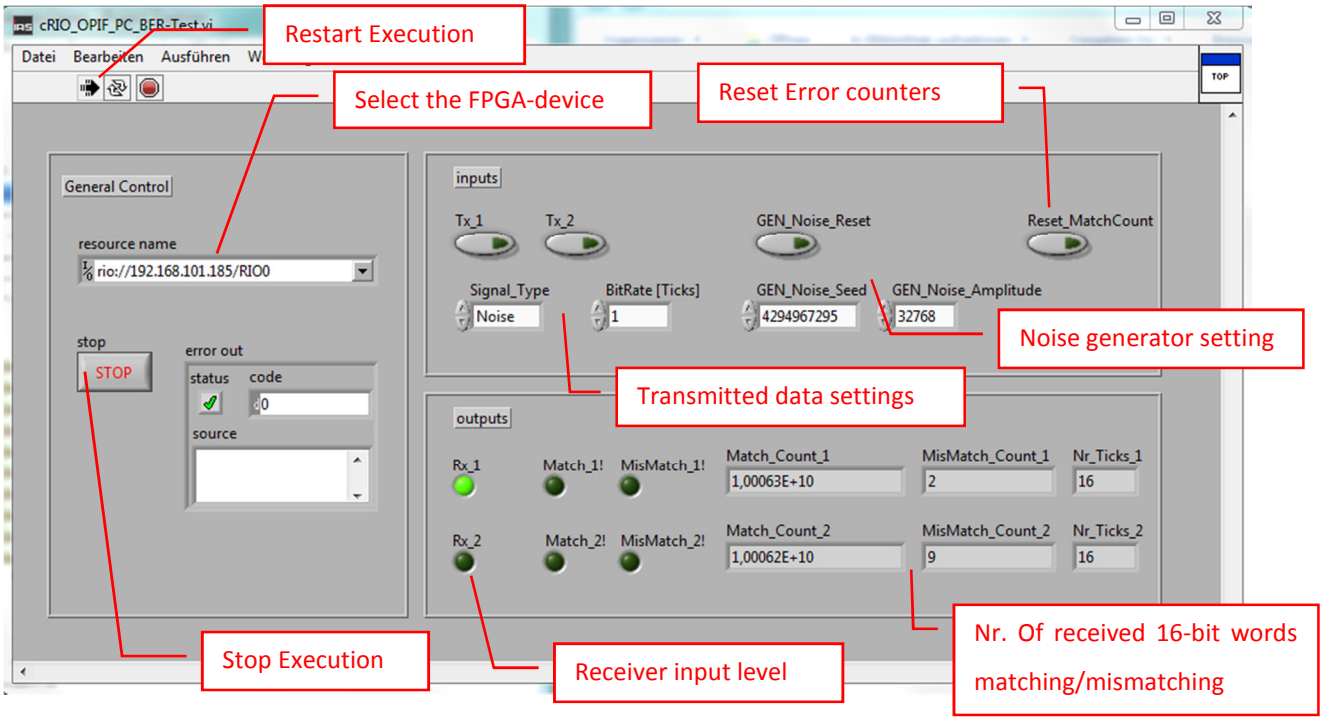


Figure 11: SW example BER-Testing

After the VI has started, PC-Software immediately tries to connect to the and the FPGA of the cRIO and will automatically run when the cRIO is available. If any system error occurs (e.g. cRIO is not available) the software stops and the erro is described in the error out indicator. Make sure, that the proper FPGA device is selected and restart execution.